Amendments to the Claims:

1. (Currently Amended) A delay equalizer for balancing clock signals in a clock tree, comprising:

a register operable to:

receive a divided input clock signal;

receive a non-divided input clock signal; and

generate a first output clock signal based on the received divided input clock signal and the received non-divided input clock signal, the first output clock signal being associated with a first delay;

a delay line operable to:

receive the non-divided input clock signal;

delay the non-divided input clock signal for a time substantially equivalent to the first delay associated with the first output clock signal; and

generate a second output clock signal being associated with a second delay substantially equal to the first delay of the first output signal; and

a multiplexer operable to:

receive the first output clock signal and the second output clock signal;

receive a select control signal indicating which of the first output clock signal or the second output clock signal to select, wherein the select control signal is programmable on the fly, and wherein the select control signal is constrained to avoid errors in clock distribution;

select either the received first output clock signal or the second output clock signal based on the select control signal; and

generate the selected first output clock signal or second output clock signal as a substantially balanced third output clock signal.

2. (Original) The delay equalizer of claim 1, wherein:

the divided clock in signal being associated with a functional mode of a device comprising the delay equalizer; and

the select control signal received by the multiplexer comprises a divided/non-divided select control signal;

the delay equalizer is operable to substantially balance the input clock signal between one or more functional modes of the device.

3. (Original) The delay equalizer of claim 2, wherein the delay equalizer is implemented at the output of existing clock dividing and selection logic.

4. (Original) The delay equalizer of claim 2, wherein the delay equalizer is implemented within existing clock dividing and selection logic, the clock dividing and selection logic being redesigned to include the delay equalizer.

5. (Original) The delay equalizer of claim 1, wherein the delay equalizer is associated with a clock-gating cell and is operable to provide the substantially balanced third output clock signal to the clock-gating cell as an input clock signal to the clock-gating cell such that an output clock signal generated by the clock-gating cell is substantially balanced.

6. (Original) The delay equalizer of claim 1, wherein:

the register comprises a flip-flop register; and

the delay line comprises one or more buffers for delaying the non-divided clock signal.

7. (Currently Amended) A method for balancing clock signals in a node of a clock tree, comprising:

receiving a divided input clock signal at a register;

receiving a non-divided input clock signal at the register;

generating at the register a first output clock signal based on the received divided input clock signal and the received non-divided input clock signal, the first output clock signal being associated with a first delay; receiving the non-divided input clock signal at a delay line;

delaying at the delay line the non-divided input clock signal for a time substantially equivalent to the first delay associated with the first output clock signal;

generating at the delay line a second output clock signal being associated with a second delay substantially equal to the first delay of the first output signal;

receiving at a multiplexer the first output clock signal and the second output clock signal;

receiving at the multiplexer a select control signal indicating which of the first output clock signal or the second output clock signal to select, wherein the select control signal is programmable on the fly, and wherein the select control signal is constrained to avoid errors in clock distribution;

selecting at the multiplexer either the received first output clock signal or the second output clock signal based on the select control signal; and

generating the selected first output clock signal or second output clock signal as a substantially balanced third output clock signal.

8. (Original) The method of claim 7, wherein:

the divided clock in signal being associated with a functional mode of a device comprising the delay equalizer; and

the select control signal received by the multiplexer comprises a divided/non-divided select control signal;

the method substantially balancing the input clock signal between one or more functional modes of the device.

9. (Original) The method of claim 8, wherein the method is performed on the output of existing clock dividing and selection logic.

10. (Original) The method of claim 8, wherein the method is integrated into existing clock dividing and selection logic, the clock dividing and selection logic having been redesigned for implementing the method.

11. (Original) The method of claim 7, further comprising providing the substantially balanced third output clock signal to a clock-gating cell as an input clock signal to the clock-gating cell such that an output clock signal generated by the clock-gating cell is substantially balanced.

12. (Original) The method of claim 7, wherein:

the register comprises a flip-flop register; and

the delay line comprises one or more buffers for delaying the non-divided clock signal.

13. (Currently Amended) A method for balancing one or more clock signals in a clock tree having a multi-mode clock distribution, comprising:

associating a first delay equalizer with at least one of a plurality of clock-gating cells arranged in one or more levels in the clock tree, the first delay equalizer operable to provide a balanced input clock signal to the clock-gating cell such that an output clock signal generated by the clock-gating cell is substantially balanced;

associating a second delay equalizer with each of one or more clock-dividing and selection modules in the clock tree, the second delay equalizer operable to substantially balance the one or more clock signals between two ~~one~~ or more functional modes;

extracting a common clock distribution topology from the clock tree, the topology accounting for substantially all of modes and clock-dividing paths of the topology;

determining one or more clock paths to be balanced, each comprising a multi-mode dependant clock path, wherein the multi-mode dependant clock path includes the two or more functional modes;

analyzing any local clock paths that were left out of the common clock distribution topology;

developing a local balancing strategy for the local clock paths that were left out of the common clock distribution topology to determine one or more constraints for substantially balancing the local clock paths;

combining the local balancing strategy with the common clock distribution to form a clock tree synthesis constraint to substantially balance the common clock distribution topology and the local clock paths in a substantially automatic process.

14. (Original) The method of claim 13, wherein determining the one or more clock paths to be balanced comprises:

determining an impact that balancing a particular clock path would have on overall clock tree balance and performance of a device associated with the clock tree;

determining whether the determined impact of the particular clock path exceeds a predetermined impact; and

if it is determined that the determined impact of balancing the particular clock path exceeds the predetermined impact, determining that the particular clock path should be balanced.

15. (Original) The method of claim 14, wherein determining an impact that balancing the particular clock path would have on the overall clock tree comprises:

determining whether the particular clock path operates asynchronously to other portions of the clock tree; and

if so, concluding that the impact of balancing the particular clock path does not exceed the predetermined impact.

16. (Original) The method of claim 13, further comprising inserting one or more exclusive-NOR (XNOR) gates throughout the clock tree to balance one or more portions of the clock tree, each XNOR gate operable to:

receive an input clock signal on an input clock path;

receive a test mode signal on a test mode path; and

generate an output clock signal on an output clock path based on an XNOR operation, a delay from the input clock path to the output clock path being independent of a delay from the test mode path to the output clock path.

17. (Original) The method of claim 16, wherein when the test mode signal received on the test mode path asserts test mode, the output clock signal generated by the XNOR gate comprises a non-inverted output clock signal.

18. (Currently Amended) A system for balancing one or more clock signals in a clock tree having a multi-mode clock distribution, comprising:

one or more first delay equalizers each associated with at least one of a plurality of clock-gating cells arranged in one or more levels in the clock tree, each first delay equalizer operable to provide a balanced input clock signal to the clock-gating cell such that an output clock signal generated by the clock-gating cell is substantially balanced;

one or more second delay equalizers each associated with each of one or more clock-dividing and selection modules in the clock tree, each second delay equalizer operable to substantially balance the one or more clock signals between two ~~one~~ or more functional modes;

the first and second delay equalizers substantially balancing the one or more clock signals in the clock tree.

19. (Original) The system of claim 18, further comprising one or more exclusive-NOR (XNOR) gates inserted throughout the clock tree to balance one or more portions of the clock tree, each XNOR gate operable to:

receive an input clock signal on an input clock path;

receive a test mode signal on a test mode path; and

generate an output clock signal on an output clock path based on an XNOR operation, a delay from the input clock path to the output clock path being independent of a delay from the test mode path to the output clock path.

20. (Original) The system of claim 19, wherein when the test mode signal received on the test mode path asserts test mode, the output clock signal generated by the XNOR gate comprises a non-inverted output clock signal.